REMARKS

This responds to the Office Action mailed on December 18, 2006.

Claims 1, 7, 10, 15 and 17 are amended, no claims are canceled, and no claims are added. As a result, claims 1-21 remain pending in this application.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §103 are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

§112 Rejection of the Claims

Claims 1-9 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant has amended independent claims 1 and 7. In claim 1, "the shared resource" of line 3 is amended into "a shared resource", and "a shared resource" of line 5 is amended into "the shared resource". In claim 7, "the cache line" of line 3 is amended into "a cache line", and "a cache line" of line 5 is amended into "the cache line". Applicant believes that such amendment to independent claims 1 and 7 overcomes the §112 rejection of claims 1-9. Applicant respectfully requests reconsideration and reversal of the §112 rejection of claims 1-9.

§103 Rejection of the Claims

Claims 1-2, 4-5, and 7-8 were rejected under 35 USC § 103(a) as unpatentable over Gilbert et al. (U.S. 6,041,376, hereinafter "Gilbert") in view of Arimilli et al. (U.S. 6,138,218, hereinafter "Arimilli").

Claims 3, 6, and 9 were rejected under 35 USC § 103(a) as unpatentable over Gilbert in view of Arimilli as applied to claims 1 and 7 above, and further in view of Donley et al. (U.S. 5,761,446, hereinafter "Donley").

Claims 10-21 were rejected under 35 USC § 103(a) as unpatentable over Vogt et al. (U.S. 5,897,656, hereinafter "Vogt") in view of Gilbert.

In the recent decision of the Supreme Court on *KSR Int'l Co. v. Teleflex Inc.*, 27 S.Ct. 1727, 82 USPQ.2d 1385 (2007), the analysis of obviousness previously set forth in *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17, 86 S.Ct. 684, 15 L.Ed.2d 545 (1966) was reaffirmed. The Court in *Graham* set out an objective analysis for applying §103, "Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject matter is determined."

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

The test for obviousness under §103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir.1985). The Examiner must, as one of the inquiries pertinent to any obviousness inquiry under 35 U.S.C. §103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990). The fact that a reference teaches away from a claimed invention is highly probative that the reference would not have rendered the claimed invention obvious to one of ordinary skill in the art. *Stranco Inc. v. Atlantes Chemical Systems, Inc.*, 15 USPQ2d 1704, 1713 (Tex. 1990). When the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious. *Id.* p. 4

citing *United States v. Adams*, 383 U.S. 39, 51-51 (1966). Additionally, critical differences in the prior art must be recognized (when attempting to combine references). *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir.1990).

Applicant traverses the rejection of these claims under 35 USC § 103(a), because the Office Action fails to establish a *prima facie* case of obviousness with respect to these claims for at least the reasons stated below.

I. Regarding the rejection of claims 1-2, 4-5, and 7-8 under 35 USC § 103(a) over Gilbert in view of Arimilli.

Regarding claim 1:

Applicant has amended claim 1, which is reproduced below (with emphasis added):

> 1. A method of preventing live-lock in a multiprocessor system, the method comprising:
> identifying a first bus transaction that is a nonmodifying transaction on a shared resource;
> identifying a second bus transaction that attempts to modify the shared resource, wherein the second bus transaction has priority over the first bus transaction to access the shared resource;
> setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending; and
> retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status bit is cleared.

Applicant submits that neither Gilbert nor Arimilli teaches a feature "the second bus transaction has priority over the first bus transaction" as recited in amended claim 1, in which "the second bus transaction" is a modifying transaction and "the first bus transaction" is a nonmodifying transaction.

Gilbert teaches using a hold flag to prevent other processors from accessing information on a node that another processor has already requested. (col. 2, ll. 43-50). Other processor requests are retried when any processor has a request for a particular resource that is first in time. (col. 3, ll 1-8). Regardless of whether the processor request is a read or a write, the procedure is the same. (col. 7, ll 5-10). In summary, according to Gilbert, all processor requests (no matter reads or writes or others) access a node on a first-come first-serve basis, and the first in time to

access the resource may set a status flag to require subsequent processor requests to be retried. (col. 2, ll. 43-50; col. 7, ll. 5-10).

Gilbert does not solve the live-lock problem as solved in the present Application. The live-lock problem occurs when a read (a non-modifying bus transaction) is accessing a resource, and a write (a modifying bus transaction) attempts to access the resource. Gilbert would allow the read to lock out the write. The processor requesting the read would then snoop the attempting write transaction and the requested data would be invalidated causing the reading processor to retry the read request. The reading processor, still in control of the resource, would begin reading again. The problem then occurs when the write request is subsequently retried. This causes the reading processor again to snoop the incoming transaction, causing the invalidation of the read data, and the cycle begins again. This cycle allows neither the read to finish reading nor the write to have access, and locks up the transactions and the resource. This is the live-lock scenario which is solved by the Application. But Gilbert does not address or solve this problem.

Claim 1 solves the live-lock problem by identifying modifying transactions (e.g. write transactions) versus nonmodifying transactions (e.g. read transactions), and offering modifying transactions priority over nonmodifying transactions. Modifying transactions are allowed to set the status bit, indicating that a bus transaction is attempting to modify the resource. Nonmodifying transactions do not set the status flag. When the status bit is set, while a bus transaction attempting to modify the resource, all other bus transactions will be retried. This includes any current read transactions operating on the resource. Rather than providing first-come first-served access to the resource, live-lock is prevented by allowing priority access to modifying bus transactions.

Because Gilbert has no concern about whether a requested operation is modifying or nonmodifying when granting the shared resource, and the requests of Gilbert are granted to access the shared resource in the order that the requests occur, in other words, first-come, first-served. Thus, it follows that Gilbert fails to show that a modifying operation (such as a "writer" operation) has priority over a nonmodifying operation (such as a "read" operation) to access the shared resource, which is positively recited in amended claim 1.

Applicant cannot find any part of Arimilli teaches the feature that the modifying bus transaction has priority over the nonmodifying bus transaction to access the shared resource. Thus, Applicant submits that neither Gilbert nor Arimilli teaches the feature that the modifying bus transaction has priority over the nonmodifying bus transaction to access the shared resource as recited in claim 1.

Further, Applicant submits that neither Gilbert nor Arimilli teaches the feature "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending" as recited in claim 1 for the reasons as stated below.

The status bit of claim 1 indicates "that a bus transaction attempting" to modify, but both Gilbert and Arimilli disclose setting a status flag after the transaction already has the resource. In claim 1, by setting the flag on an attempt to modify, the modifying bus transaction can set the flag even though another nonmodifying bus transaction has control of the resource.

Referring to Gilbert, column 2, line 52-56 (with emphasis added):

> "In one aspect of the invention, a remote cache interconnect (also called a network controller) within a node has access to a hold flag. The remote cache interconnect sets or activates the hold flag when it receives data from the system interconnect for delivery to a requesting processor."

It can be seen that Gilbert describes a hold flag, which is used to indicate that a remote cache has received data, and not for "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending" as recited in claim 1. Clearly, the hold flag of Gilbert and the status bit of claim 1 are different approaches for different purposes.

Further referring to Arimilli, column 3, lines 5-12 (with emphasis added):

> "When a device snooping the system bus of a multiprocessor system detects an operation requesting data which is resident within a local memory in a coherency state requiring the data to be sourced from the device, the device attempts a intervention. If the intervention is impeded by a second device asserting a retry, the device sets a flag to provide historical information regarding the failed intervention."

It can be seen that Arimilli discloses setting a bit as a historical information regarding a failed intervention, and not for "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending" as recited in claim 1. Clearly, the flag of Arimilli and the status bit of claim 1 are different approaches for different purposes.

Therefore, Applicant submits that neither Gilbert nor Arimilli teaches the feature "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending" as recited in claim 1.

Accordingly, Applicant respectfully submits that Gilbert and Arimille, either alone or in combination, fail to teach or suggest "the second bus transaction has priority over the first bus transaction" or "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending" as recited in amended claim 1, thus the cited references fail to teach or suggest all the elements of rejected claim 1. Thus, Applicant respectfully submits that the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 1. Applicant respectfully requests reconsideration and allowance of claim 1.

Regarding claim 7:

The arguments above regarding claim 1 also apply to claim 7. Additionally, claim 7 further clarify how the claimed invention does not follow the strict first-come first-served process of Gilbert. Gilbert does not describe any system where a bus transaction which has been granted a resource may be forced to retry as an incoming bus transaction steps in and sets a status flag to keep claim the resource or cache line.

Thus, Applicant respectfully submits that Gilbert and Arimille, either alone or in combination, fail to teach or suggest all the elements in rejected claim 7. Thus, Applicant respectfully submits that the Office Action fails to establish a *prima facie* case of obviousness with respect to claim 7. Applicant respectfully requests reconsideration and allowance of claim 7.

Regarding claims 2, 4-5 and 8:

Claims 2 and 4-5 depend from claim 1. Claim 8 depends from claim 7. The arguments discussed for claims 1 and 7 also apply to these dependent claims. Thus, Applicant respectfully submits that the Office Action fails to establish a *prima facie* case of obviousness with respect to claims 2, 4-5 and 8. Applicant respectfully requests reconsideration and allowance of claims 2, 4-5 and 8.

II. Regarding the rejection of claims 3, 6 and 9 under 35 USC § 103(a) over Gilbert in view of Arimilli and Donley.

Claims 3, 6 and 9 depend respectively from claims 1 and 7, thus include all the elements of the independent claim from which they depend. For at least the reasons discussed above for claims 1 and 7, Applicant respectfully submits that neither Gilbert nor Arimilli teaches or suggests all the elements of claims 3, 6 and 9. The Office Action relies on Donley to supply these missing elements. Therefore, Applicant submits neither Gilbert, nor Arimilli, nor Donely, alone or in combination, recites all the elements of claims 3, 6 and 9. Hence, the Office Action fails to establish a *prima facie* case of obviousness with respect to claims 3, 6 and 9. Therefore, Applicant respectfully requests reconsideration and allowance of claims 3, 6 and 9.

III. Regarding the rejection of claims 10-21 under 35 USC § 103(a) over Vogt in view of Gilbert.

Regarding Claims 10, 15 and 17:

Independent claims 10 and 15 each recite, "a status indicator associated with each one of the plurality of buffers, the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the shared resource" or "system memory." Independent claim 17 recites, "a plurality of status indicators being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the one of the cache line." These claims further clarify the novelty of the Application, and more visibly illustrate the differences between the references cited in the Office Action. The Office Action relies on Vogt and Gilbert. The arguments presented above regarding claim 1 with regard to Gilbert also apply to these claims. Additionally, neither Gilbert nor Vogt, either alone or in combination, teaches or suggests all of the elements of claims 10, 15 or 17. Specifically, at a minimum, neither reference describes the elements presented above in this paragraph.

Thus, Applicant respectfully submits that the Office Action fails to establish a *prima facie* case of obviousness with respect to claims 10, 15 and 17. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 10, 15 and 17.

Regarding Claims 11-14, 16 and 18-21:

Claims 11-14, 16, and 18-21 depend from independent claims 10, 15 and 17 respectively, thus include all the elements of the independent claim from which they depend. For at least the

reasons discussed above for independent claims 10, 15 and 17, Applicant respectfully submits that the Office Action fails to establish a *prima facie* case of obviousness with respect to claims 11-14, 16 and 18-21. Therefore, Applicant respectfully requests reconsideration and allowance of claims 11-14, 16, and 18-21.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6900 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

BRIAN R. BENNETT ET AL.

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 373-6900

Date 6/18/2007

By _____
Jun Wei
Reg. No. 55,717

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 18th day of June 2007.

Amy Moriarty
Name

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Signature